

## MARKED UP VERSION

24. (amended) A semiconductor device formed by the method [of claim 21]  
comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the  
monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming  
adjacent to said surface an amorphous layer of the semiconductor material, said  
amorphous semiconductor layer extending to a substantially planar zone disposed at  
substantially said selected depth and comprising monocrystalline semiconductor material  
damaged by lattice defects, undamaged monocrystalline semiconductor material below  
said selected depth comprising a first layer of the monocrystalline semiconductor  
material;

heating said wafer under conditions effective to convert said amorphous  
semiconductor layer to a second layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of  
monocrystalline semiconductor material damaged by lattice defects, thereby forming a  
substantially planar intrinsic gettering zone comprising substantially pure semiconductor  
material and including active gettering sites, said gettering zone being disposed  
substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and  
bonding said insulating bond layer to said surface of said wafer, thereby forming a  
bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating  
bond layer, and a monocrystalline semiconductor device wafer, said device wafer  
containing a substantially planar intrinsic gettering zone that comprises substantially pure  
semiconductor material and includes active gettering sites;

forming a semiconductor device on said second layer of  
monocrystalline semiconductor material or on layer of epitaxial monocrystalline  
semiconductor material deposited on said second layer, and

wherein the said semiconductor device is formed on said epitaxial layer.

26. (amended) A semiconductor device formed by the process [of claim 23] comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below said selected depth comprising a first layer of the monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a second layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions;

wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide; and

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**PAGE 10**

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**Title: BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANER  
INTRISTIC GETTERING ZONE**

forming a semiconductor device on said bonded substrate.

30. (amended) The substrate of claim 28 wherein said monocrystalline semiconductor material comprises silicon [and said implanted ions comprise silicon ions] implanted with silicon ions.